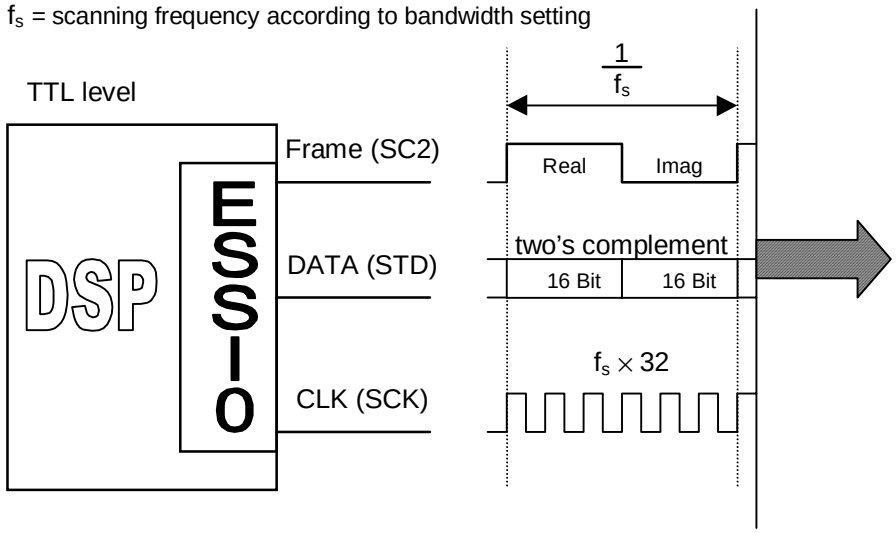
Annex I (Digital IF Output)

Digital IF output at the unit's rear panel.

The EB200 makes the digital IF signal available at the rear panel. In order to receive the IQ signal, the "demodulation kind" of the receiver must be set to "IQ". The output signal is demodulated and in the position AGC it is preregulated.

The data are serially output at termial X6 (Option) by means of SFRAME (pin 12), SCLOCK (pin 24) and SDATA (pin 25). These three lines are driven by a 74LVC245 supplied with 3,3 V through a 100-ohm series resistance for each line. Therefore the external line length should not exceed 20 cm. If longer lines are necessary, corresponding transmission drivers should be planned directly at the output of the unit.

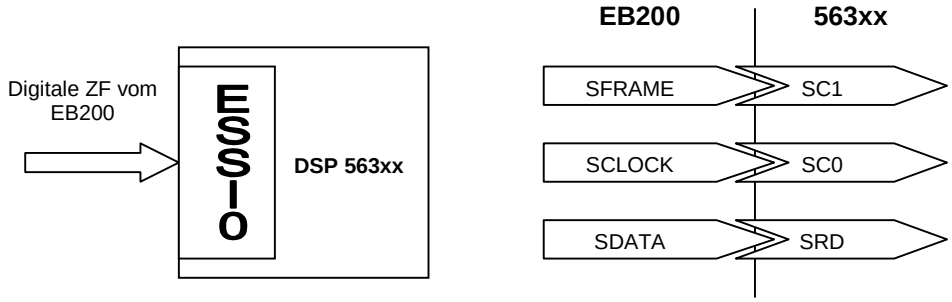


Bandwidths and scanning rates

Scanning frequency f_s	**IF bandwidth**	**Data rate MBit/s**
256 kHz	150kHz, 120kHz	8.192
128 kHz	50kHz	4.096
64 kHz	30kHz	2.048
32 kHz	15kHz	1.024
16 kHz	9kHz, 6kHz	0.512
4 kHz	2.4kHz, 1.5kHz	0.128
2 kHz	1kHz	0.064
1 kHz	600Hz	0.032
0.5 kHz	300Hz	0.016
0.25 kHz	150Hz	0.008

Data output via a DSP of the Motorola 563xx-family.

If the digital IF-output should be read-out by means of a second DSP of the Motorola 563xx-family it can happen as follows:



Configuration of the ESSI0 in the DSP 563xx

- ***asynchron***
- ***network mode***
- ***frame sync polarity = 0***
- ***frame sync relative timing = 0***
- ***frame sync length = WORD***
- ***clock polarity = 0***

```
Assembler-Code:
movep    #$0,x:M_PCRC    ; Reset ESSI0
movep #>%000000000010000000011000,x:<<M_CRB0
movep #>%000100000010000000000000,x:<<M_CRA0
movep   #$3C,x:M_PCRC
bset    #17,x:M_CRB0      ;ESSI0 enable
```

Data output to a personal computer

If the data processing as depicted below is not directly carried out by a Motorola DSP then, for example, at first an FPGA can receive the data stream and then pass it on to other processors.